Electronic Circuit Diagrams in GLE

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1 Introduction

This document is intended to provide some basic documentation for the use of `electronics.gle` for drawing circuit diagrams. It is currently a bit basic, but will hopefully be added to at a later date.

2 Functions

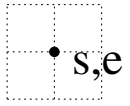
The following is a list of all the functions available, along with their options. The meanings of the various options will (hopefully) become self-explanatory with the examples that follow in the next section.

```
@connection
@resistor_h rlabel$
@resistor_v rlabel$
@potentiometer_hb rlabel$
@potentiometer_vr rlabel$
@vresistor_h rlabel$
@vresistor_v rlabel$
@npn_bjt bjtlabel$
@pnp_bjt bjtlabel$
@n_mosfet mlabel$
@p_mosfet mlabel$
@igbt igbtlabel$
@inductor_h core ilabel$
@inductor_v core ilabel$
@xformer core type
@xformer_dblsecondary type location
@p_capacitor polarity
```

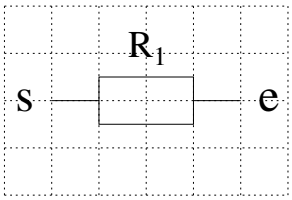
```
@p_capacitor_hl clabel$
@p_capacitor_hr clabel$
@p_capacitor_vt clabel$
@p_capacitor_vb clabel$
@capacitor_h clabel$
@capacitor_v clabel$
@vcapacitor_h clabel$
@vcapacitor_v clabel$
@diode_hr dlabel$
@diode_hl dlabel$
@diode_vd dlabel$
@diode_vu dlabel$
@bridge_rectifier blabel$
@opamp supply ulabel$
@ground
@supply_h type
@supply_v type
@cell_h elabel$
@cell_v elabel$
@and
@nand
@or
@nor
@xor
@xnor
@not
@buffer
```

3 Symbols

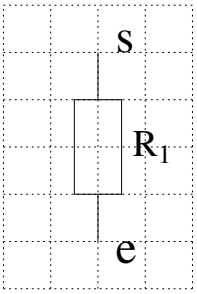
This section gives a list of the various symbols that can be produced with the provided functions. The symbol 's' refers to the start point for drawing and 'e' refers to the end point.



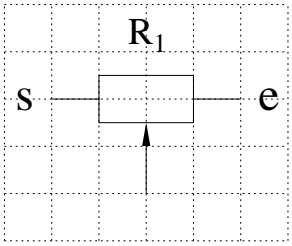

```
amove 1 1
@connection
```



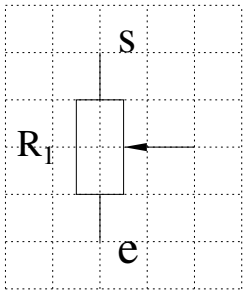

```
amove 1 2
@resistor_h "R_1"
```



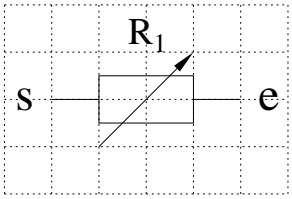

```
amove 2 5
@resistor_v "R_1"
```



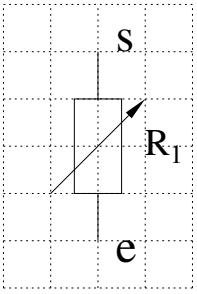

```
amove 1 3
@potentiometer_hb "R_1"
```



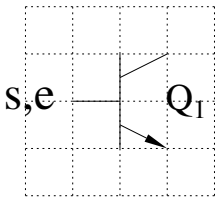

```
amove 2 5
@potentiometer_vr "R_1"
```



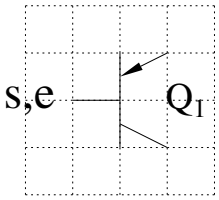

```
amove 1 2
@vresistor_h "R_1"
```



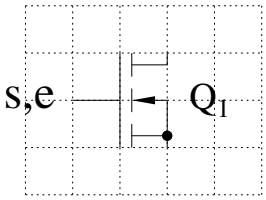

```
amove 2 5
@vresistor_v "R_1"
```



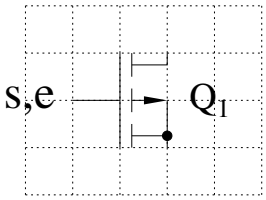

```
amove 1 2
@npn_bjt "Q_1"
```



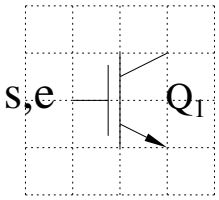

```
amove 1 2
@pnp_bjt "Q_1"
```



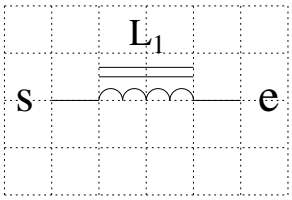

```
amove 1 2
@n_mosfet "Q_1"
```



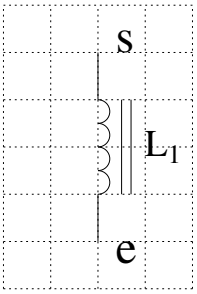

```
amove 1 2
@p_mosfet "Q_1"
```



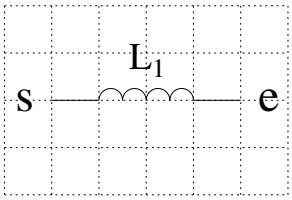

```
amove 1 2
@igbt "Q_1"
```



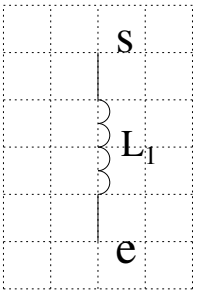

```
amove 1 2
@inductor_h 1 "L_1"
```



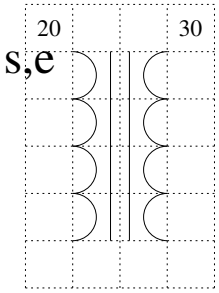

```
amove 2 5
@inductor_v 1 "L_1"
```



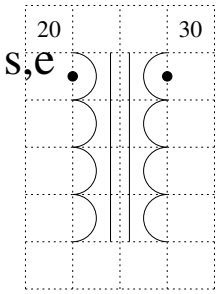

```
amove 1 2
@inductor_h 0 "L_1"
```



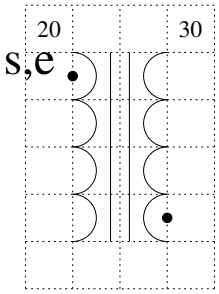

```
amove 2 5
@inductor_v 0 "L_1"
```



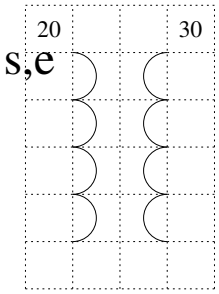

```
amove 1 5
@xformer 1 0 "20" "30"
```



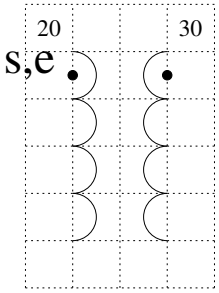

```
amove 1 5
@xformer 1 1 "20" "30"
```



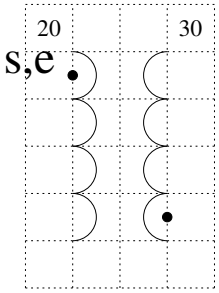

```
amove 1 5
@xformer 1 2 "20" "30"
```



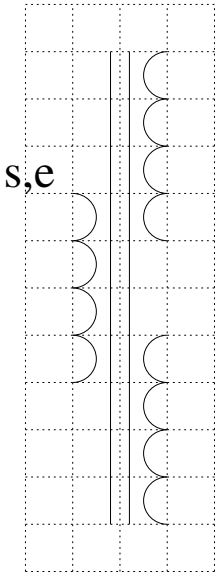

```
amove 1 5
@xformer 0 0 "20" "30"
```



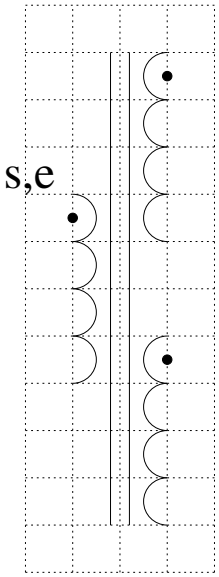

```
amove 1 5
@xformer 0 1 "20" "30"
```



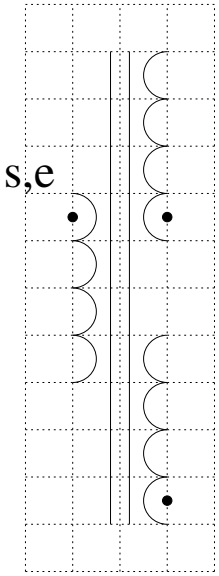

```
amove 1 5
@xformer 0 2 "20" "30"
```



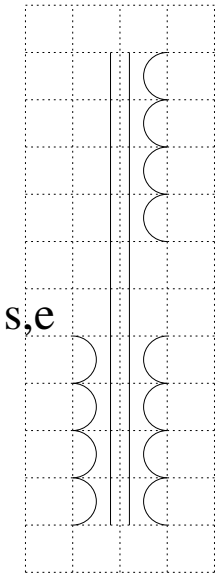

```
amove 1 8
@xformer_dblsecondary 0 0
```



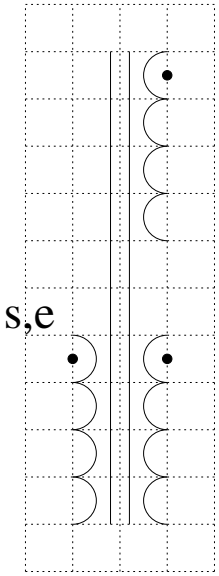

```
amove 1 8
@xformer_dblsecondary 1 0
```



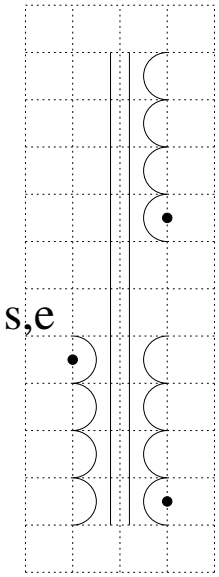

```
amove 1 8
@xformer_dblsecondary 2 0
```



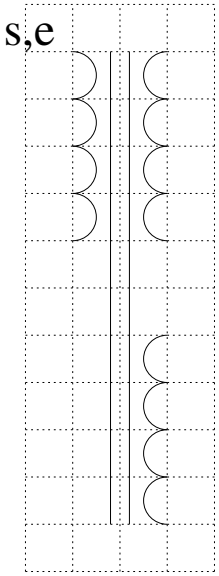

```
amove 1 5
@xformer_dblsecondary 0 1
```



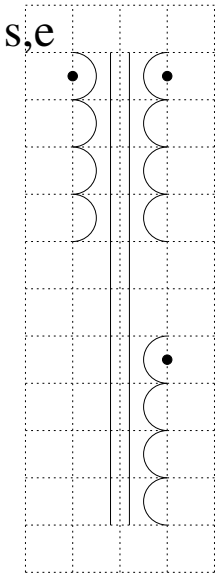

```
amove 1 5
@xformer_dblsecondary 1 1
```



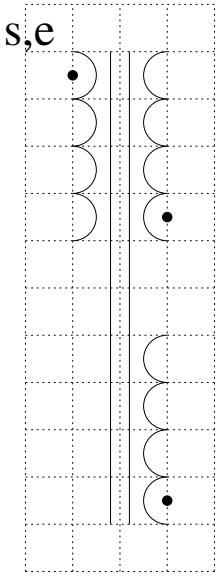

```
amove 1 5
@xformer_dblsecondary 2 1
```



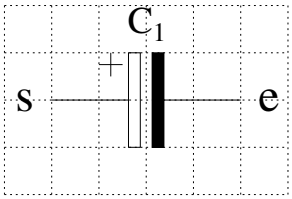

```
amove 1 11
@xformer_dblsecondary 0 2
```



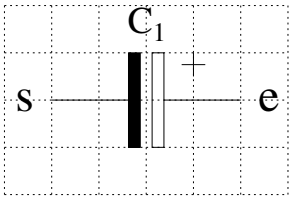

```
amove 1 11
@xformer_dblsecondary 1 2
```



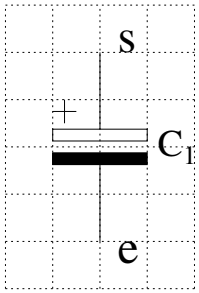

```
amove 1 11
@xformer_dblsecondary 2 2
```



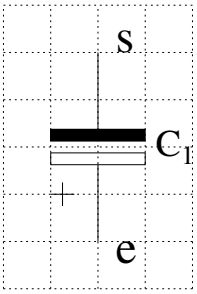

```
amove 1 2
@p_capacitor_hl "C_1"
```



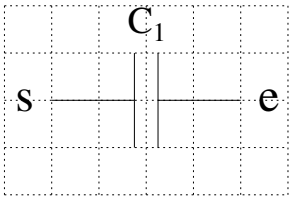

```
amove 1 2
@p_capacitor_hr "C_1"
```



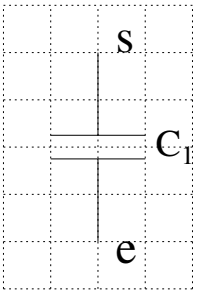

```
amove 2 5
@p_capacitor_vt "C_1"
```



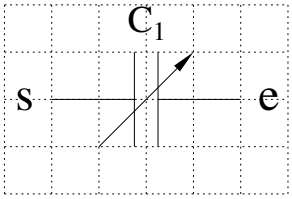

```
amove 2 5
@p_capacitor_vb "C_1"
```



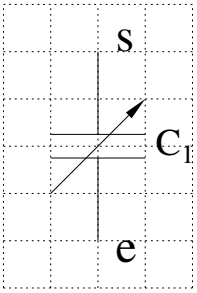

```
amove 1 2
@capacitor_h "C_1"
```



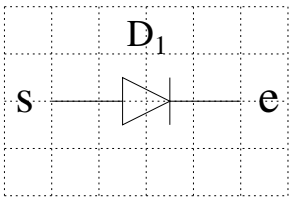

```
amove 2 5
@capacitor_v "C_1"
```



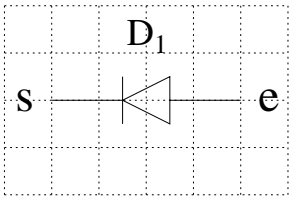

```
amove 1 2
@vcapacitor_h "C_1"
```



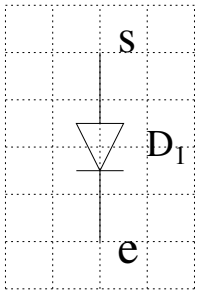

```
amove 2 5
@vcapacitor_v "C_1"
```



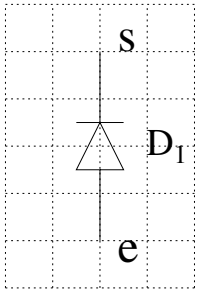

```
amove 1 2
@diode_hr "D_1"
```



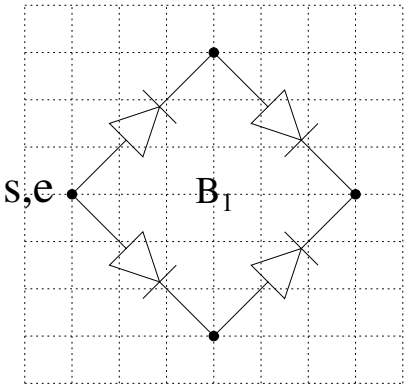

```
amove 1 2
@diode_hl "D_1"
```



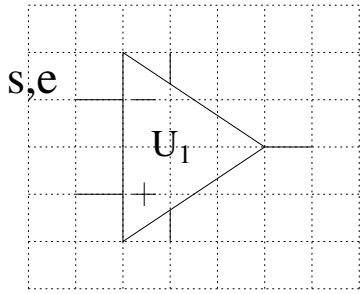

```
amove 2 5
@diode_vd "D_1"
```



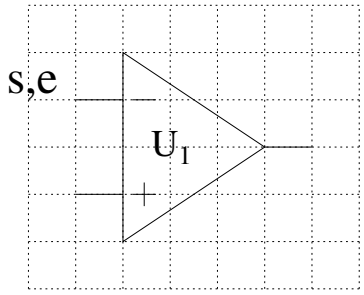

```
amove 2 5
@diode_vu "D_1"
```



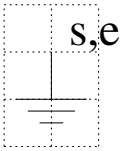

```
amove 1 4
@bridge_rectifier "B_1"
```



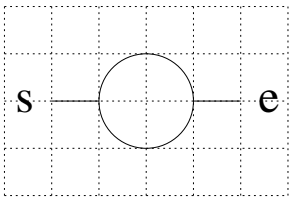

```
amove 1 4
@opamp 1 "U_1"
```



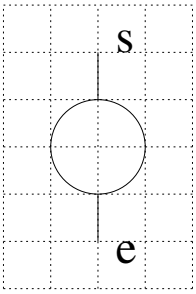

```
amove 1 4
@opamp 0 "U_1"
```



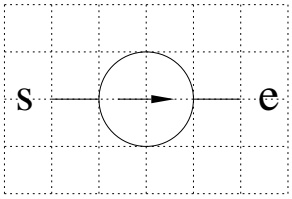

```
amove 1 2
@ground
```



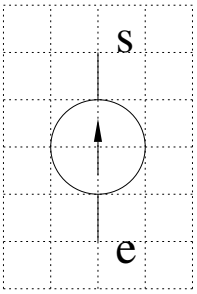

```
amove 1 2
@supply_h 0
```



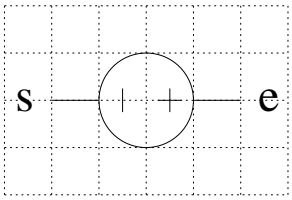

```
amove 2 5
@supply_v 0
```



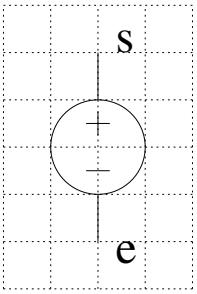

```
amove 1 2
@supply_h 1
```



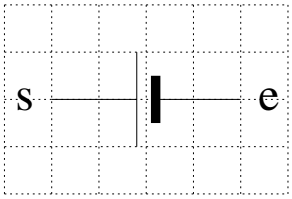

```
amove 2 5
@supply_v 1
```



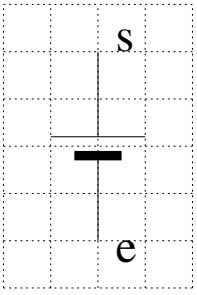

```
amove 1 2
@supply_h 2
```



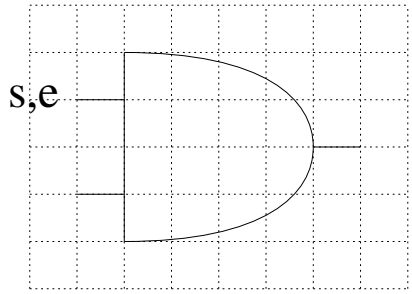

```
amove 2 5
@supply_v 2
```



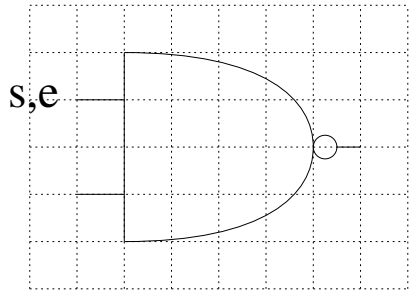

```
amove 1 2
@cell_h "E_1"
```



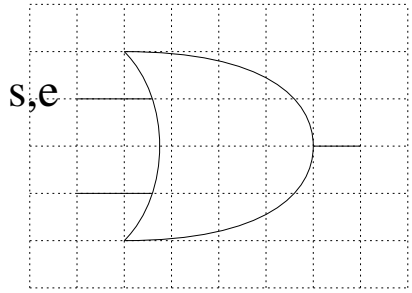

```
amove 2 5
@cell_v "E_1"
```



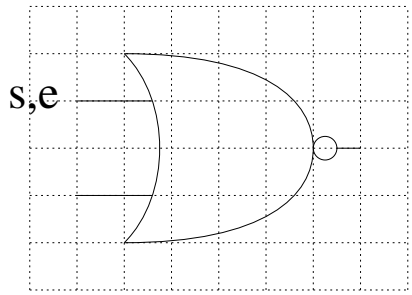

```
amove 1 4
@and
```



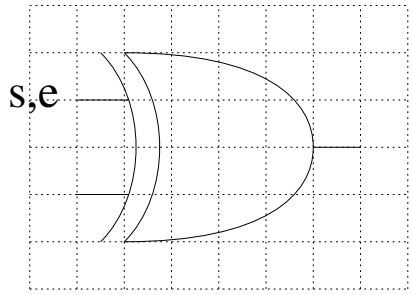

```
amove 1 4
@nand
```



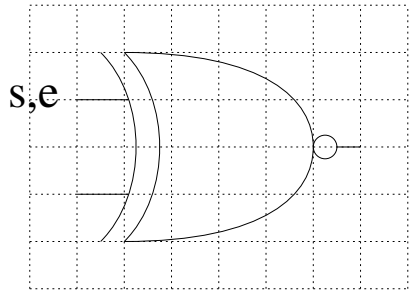

```
amove 1 4
@or
```



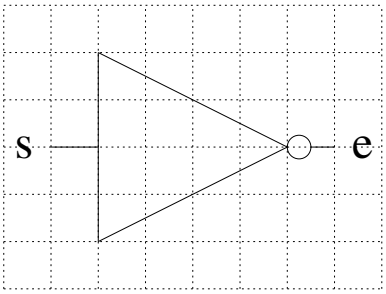

```
amove 1 4
@nor
```



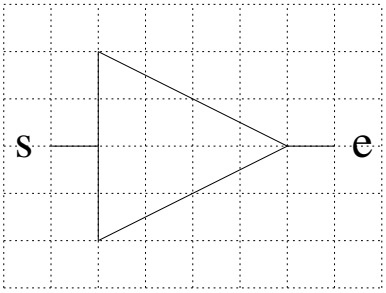

```
amove 1 4
@xor
```




```
amove 1 4
@xnor
```



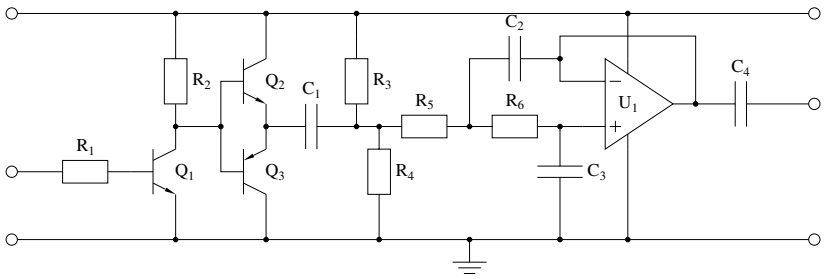

```
amove 1 3
@not
```




```
amove 1 3
@buffer
```

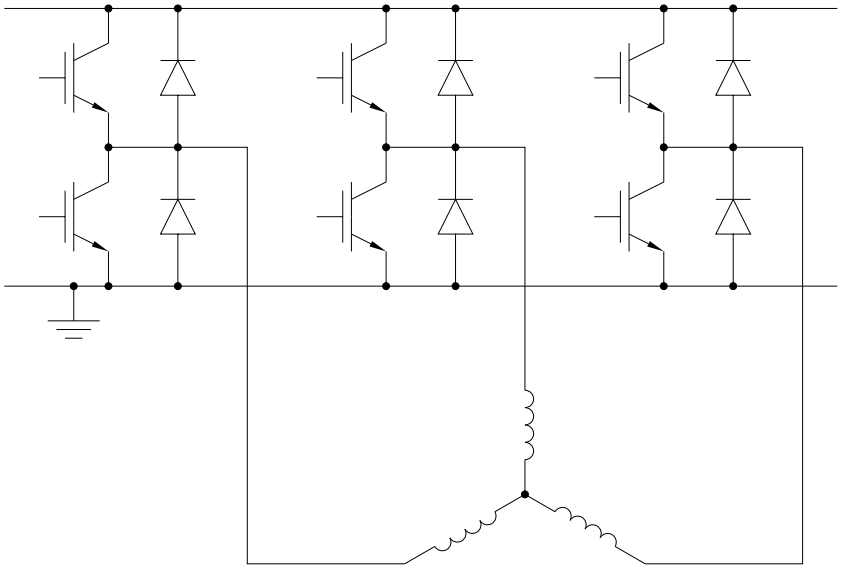
4 Examples

This section gives a few examples of real circuits that have been drawn with this package.



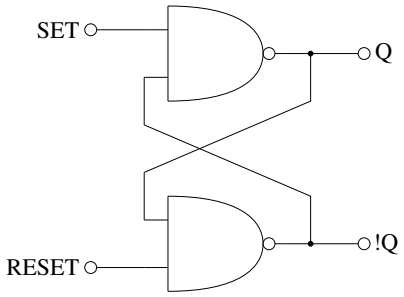
```
! Example circuit with electronics.gle
size 20 7.5
include electronics.gle


begin scale 0.5 0.5

    termrad = 0.25
    amove 1 3
    rmove -termrad 0
    circle termrad
    rmove termrad 0

    rline 35 0
    rmove termrad 0
    circle termrad
    amove 1 6
    rmove -termrad 0
    circle termrad
    rmove termrad 0
    rline 1 0
    @resistor_h "R_1"
    @npn_bjt "Q_1"
    rmove 2 -1
    rline 0 -2
    @connection
    rmove 0 4
    rline 0 1
    @connection
    rmove 0 5
    @connection
    rline 0 -1
    @resistor_v "R_2"
    rline 2 0
    @connection
    rline 0 2
    @npn_bjt "Q_2"
    rmove 0 -2
    rline 0 -2
    @pnp_bjt "Q_3"
    rmove 2 -1
    rline 0 -2
    @connection
    rmove 0 4
    rline 0 2
    rmove 0 2
    rline 0 2
    @connection
    rmove 0 -5
    @connection
    @capacitor_h "C_1"
    rmove 0 5
    @connection
    rline 0 -1
    @resistor_v "R_3"
    @connection
    rline 1 0
    @connection
    resistor_v "R_4"
    rline 0 -1
    @connection
    rmove 0 5
```

```
    @resistor_h "R_5"
    @connection
    gsave
    @resistor_h "R_6"
    @connection
    rline 1 0
    rmove -1 0
    @capacitor_v "C_3"
    rline 0 -1
    @connection
    grestore
    rline 0 3
    @capacitor_h "C_2"
    @connection
    rline 0 -1
    rline 1 0
    gsave
    @opamp 1 "U_1"
    rmove -1 1
    rline 0 1
    rline 6 0
    rline 0 -3
    @connection
    @capacitor_h "C_4"
    rline 1 0
    rmove termrad 0
    circle termrad
    rmove -termrad 0
    grestore
    rmove 2 1
    rline 0 2
    @connection
    rmove 0 -6
    rline 0 -4
    @connection
    rmove -7 0
    @connection
    @ground

    amove 1 13
    rmove -termrad 0
    circle termrad
    rmove termrad 0
    rline 35 0
    rmove termrad 0
    circle termrad
    rmove -termrad 0
end scale
```



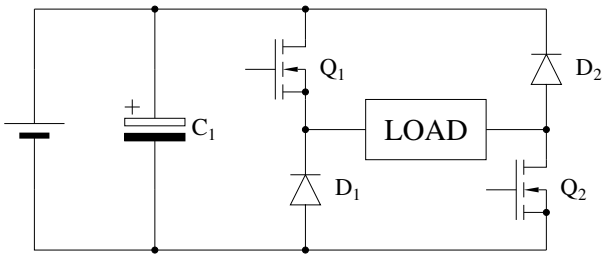
```
! Three-phase inverter
size 13 10

include electronics.gle


begin scale 0.5 0.5

    ! Draw the DC Link
    amove 1 19
    rline 24 0

    ! Draw Ground
    amove 1 11
    rline 2 0
    @connection
    @ground
    rline 22 0

    ! Transistors
    for i = 0 to 16 step 8
        for j = 0 to 4 step 4
            amove 2 13
            rmove i j
            @igbt ""
            rmove 2 1
            rline 0 1
            rmove 0 -3
            rline 0 -1
            rmove 2 4
            @diode_vu ""
        next j
    next i
```

```
    ! Connection points
    amove 4 11
    for i = 0 to 16 step 8
        for j = 0 to 8 step 4
            amove 4 11
            rmove i j
            @connection
            rmove 2 0
            @connection
        next j
    next i

    ! Machine windings
    amove 12 15
    rline 4 0
    rline 0 -6
    @inductor_v 0 ""
    @connection
    star_x = xpos()
    star_y = ypos()
    begin rotate -30
        @inductor_h 0 ""
    end rotate
    rmove 4*cos(torad(30)) -4*sin(torad(30))
    end_y = ypos()
    aline 24 end_y
    aline 24 15
    rline -4 0
    amove star_x star_y
    begin rotate 210
        @inductor_h 0 ""
    end rotate
    rmove -4*cos(torad(30)) -4*sin(torad(30))
    aline 8 end_y
    aline 8 15
    rline -4 0

end scale
```




```
! Example of logic gate use: SR Flip-Flop

size 19 14
```

```
include electronics.gle

! Radius of end terminals
termrad = 0.25

! Reset input
amove 4 2
rmove -termrad 0
circle termrad
rmove -2*termrad 0
set just RC
text RESET
rmove 3*termrad 0
rline 2 0

! Set input
amove 4 12
rmove -termrad 0
circle termrad
rmove -2*termrad 0
set just RC
text SET
rmove 3*termrad 0
rline 2 0

! Top NAND Gate
@nand
rmove 0 -2
rline 0 -2
rmove 0 -2
rline 0 -2
! Bottom NAND Gate
@nand

! Interconnections
rmove 6 -1
rline 1 0
@connection
rline 0 2
rline -7 3
rmove 0 -2
rline 7 3
rline 0 2
@connection
rline -1 0
rmove 1 0

! Top Output
rline 2 0
rmove termrad 0
circle termrad
rmove 2*termrad 0
set just LC
text Q

! Bottom Output
rmove 0 -8
text !Q
rmove -2*termrad 0
circle termrad
rmove -termrad 0
rline -2 0
```




```
! An H-Bridge

! Set the page size
size 21 10

! Import the electronics module
include electronics.gle

! Draw a grid if the line below is uncommented
!@drawgrid xscale

! Top left of diagram
amove 2 9
gsave

! Battery leg
rline 0 -2
@cell_v "E_1"
rline 0 -2

! Ground plane
rline 17 0

! Return to top left
grestore

! Power to cap leg
rline 4 0
@connection
rline 0 -2
@p_capacitor_vt "C_1"
rline 0 -2
@connection

! Back to power rail
rmove 0 8

! Power to First Leg
rline 5 0
@connection
rline 0 -1
rmove -2 -1
@n_mosfet "Q_1"
rmove 2 -1
rline 0 -1
```

```
@connection
@diode_vu "D_1"
@connection

! Back to Power rail
rmove 0 8

! Power to second leg
rline 8 0
@diode_vu "D_2"
@connection
rline 0 -1
rmove -2 -1
@n_mosfet "Q_2"
rmove 2 -1
rline 0 -1

! Back to right hand side of load
rmove 0 4

! Connections to load
rline -2 0
rmove -4 0
rline -2 0
rmove 2 -1

! Load
box 4 2
rmove 2 1
set just CC
text LOAD
```
